



High Temperature Static RAM, 4 Megabit (256K X 16)

FEATURES

- Operation to 200°C
- Single 2.7V ~ 5.5V power supply
- Asynchronous Operation
- Low power consumption
- All outputs TTL compatible
- Completely static memory
- Tri-state output
- Popular 50-pin PGA footprint

APPLICATIONS

- High temperature Digital System applications
- Downhole applications
- Avionics
- Automotive applications

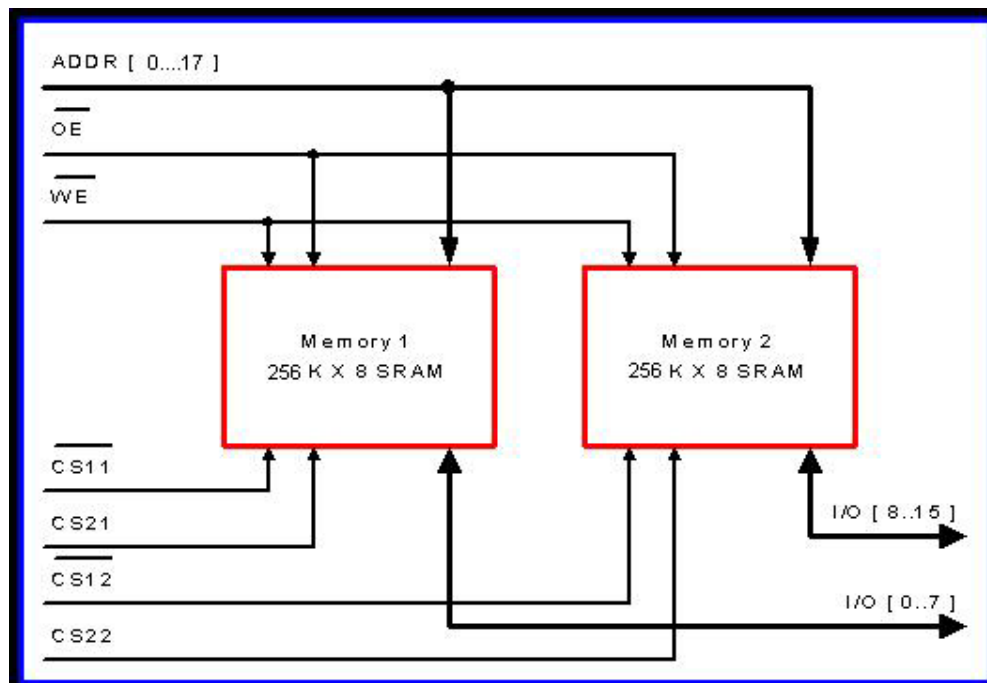
DESCRIPTION

The TX5305 is a CMOS static RAM organized as 262,144 x 16-bit words. The device is packaged in a proprietary 50-pin ceramic PGA package employing the 5 x 10 pin footprint with a pitch of 0.1 inch. Powered by a single 2.7V ~ 5 V supply, the unit offers low standby power dissipation and is suitable for battery backup systems. Output lines are tri-stated; power consumption can be minimized through use of the data retention mode.

The TX5305 is composed of two individual SRAM modules, each with 256K x 8-bit memory. Each module has private enable/select lines permitting store/ access of either 8-bit or 16-bit data.

The TX5305 operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible. The TX5305 is designed for use in systems operating in very high temperature environments.

TX5305 FUNCTIONAL BLOCK DIAGRAM



TX5305 – Specifications

ABSOLUTE MAXIMUM RATINGS*

| Parameter | Symbol | Value | Unit |
|---|-----------|------------------------|------|
| Supply Voltage relative to V_{SS} | V_{CC} | -0.5 to + 5.5 | V |
| Voltage on any pin relative to V_{SS} | V_T | -0.5 to $V_{CC} + 0.5$ | V |
| Operating Temperature Range | T_{opr} | 0 to + 200 | °C |
| Storage Temperature Range | T_{stg} | -55 to + 200 | °C |
| DC Output Current | I_{out} | 50 | mA |

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|--------------------|----------|------|----------------|------|
| Supply Voltage | V_{CC} | 2.7 | 5.5 | V |
| Ground Voltage | V_{SS} | 0.0 | 0.0 | V |
| Input High Voltage | V_{IH} | 2.4 | $V_{CC} + 0.2$ | V |
| Input Low Voltage | V_{IL} | -0.2 | 0.6 | V |

DC ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Value (typ) | Unit |
|---|-----------|-------------|---------|
| Input Leakage Current, $V_{CC} \cong V_{IN} \cong V_{SS}$ | I_{LI} | 2.0 | μA |
| Output Leakage Current | I_{LO} | 2.0 | μA |
| Operating Supply Current | I_{CC} | 60 | mA |
| Standby Supply Current | I_{SB1} | 1.0 | mA |
| Data Retention Supply Current, $V_{CC} = 3.0$ | I_{DR} | 0.2 | μA |
| $V_{CC} = 2.0$ | I_{DR} | 0.2 | μA |
| Output Voltage Low | V_{OL} | 0.4 | V |
| Output Voltage High | V_{OH} | 2.4 | V |
| V_{CC} for data retention | V_{DR} | 1.5 | V |
| Chip deselect to data retention time | t_{CDR} | 0 | ns |
| Read Cycle Time | t_{RC} | 70 | ns |
| Write Cycle Time | t_{WC} | 70 | ns |
| Input Capacitance | C_{IN} | 6 | pF |
| Input/Output Capacitance | $C_{I/O}$ | 8 | pF |

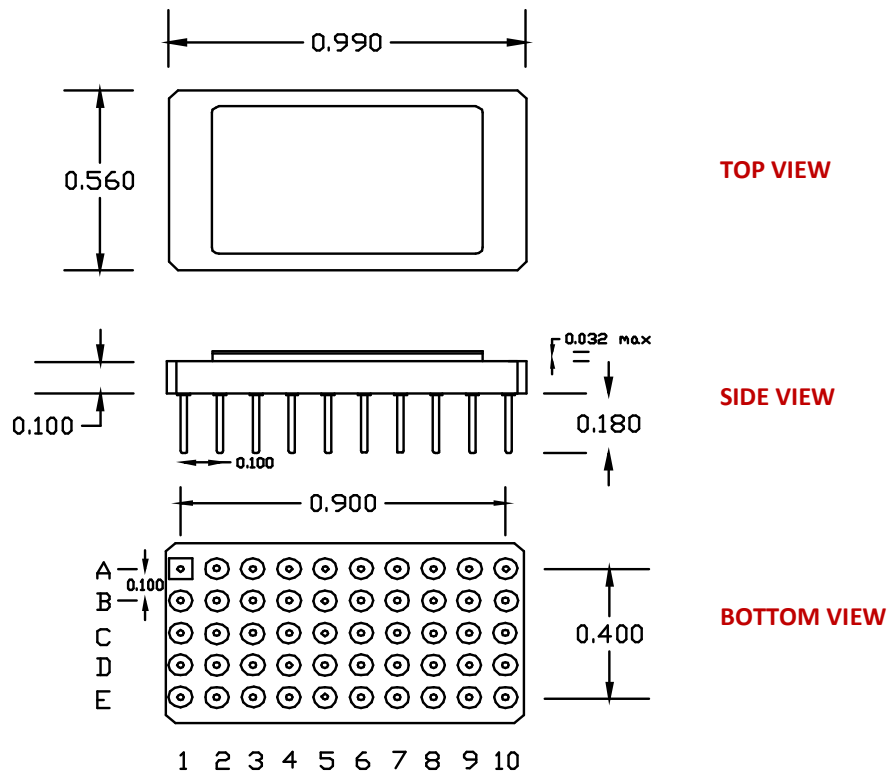
TX5305 PACKAGE INFORMATION

TRUTH TABLE

For 256K x 16 bit operation

| Mode | CS21/CS22 | CS11/CS12 | *WE | *OE | I/O Pin | Supply Current |
|----------------|-----------|-----------|-----|-----|-------------|----------------|
| Not Selected | L | X | X | X | High-Z | Standby |
| Not Selected | X | H | X | X | High-Z | Standby |
| Output Disable | H | L | H | H | High-Z | Active |
| Read | H | L | H | L | Data Output | Active |
| Write | H | L | L | X | Data Input | Active |

H = High Voltage, L = Low Voltage, X = Don't Care



TX5305 PACKAGE PIN INFORMATION

| | A | B | C | D | E |
|----|-----------------|------|------------------------|--------------------------|--------------------------|
| 1 | N.C. | A17 | N.C. | N.C. | $\overline{\text{CE12}}$ |
| 2 | V _{ss} | N.C. | N.C. | CS22 | V _{cc} |
| 3 | N.C. | A16 | $\overline{\text{WE}}$ | CS21 | A15 |
| 4 | A14 | A12 | A7 | A8 | A13 |
| 5 | A6 | A5 | $\overline{\text{OE}}$ | A11 | A9 |
| 6 | A4 | A3 | A2 | $\overline{\text{CE11}}$ | A10 |
| 7 | A1 | A0 | I/O13 | I/O12 | I/O11 |
| 8 | I/O10 | I/O9 | I/O8 | I/O15 | I/O14 |
| 9 | V _{ss} | I/O1 | I/O3 | I/O5 | V _{cc} |
| 10 | I/O0 | I/O2 | I/O4 | I/O6 | I/O7 |

WARNING! Static Sensitive Device.

The TX5305 is a hybrid network that includes several sensitive components. These components can be damaged or destroyed by discharge of static electricity. The discharge of static electricity is commonly referred to as Electrostatic Discharge (ESD).

The TX5305 can be protected from ESD by the following common procedures used with discrete semiconductors, namely:

1. Always store units in closed conductive containers
2. All personnel that handle units must wear static dissipative outer garments and must be electrically grounded
3. Always use a grounded soldering iron when making electrical connections
4. Worktables must have grounded dissipative covering.

ESD can cause subtle problems that have longer term, damaging affect.