2- Megabit (128K X 16) High-Temperature Static RAM

FEATURES

- Operation to 200°C
- Popular 50-pin PGA footprint
- Single 5 V supply
- Robust Geometry
- Access time : 100 ns at rated temperature
- Completely static memory
- (128K x 16 bit) or (2 128K x 8 bit) organization
- Tri-state output

APPLICATIONS

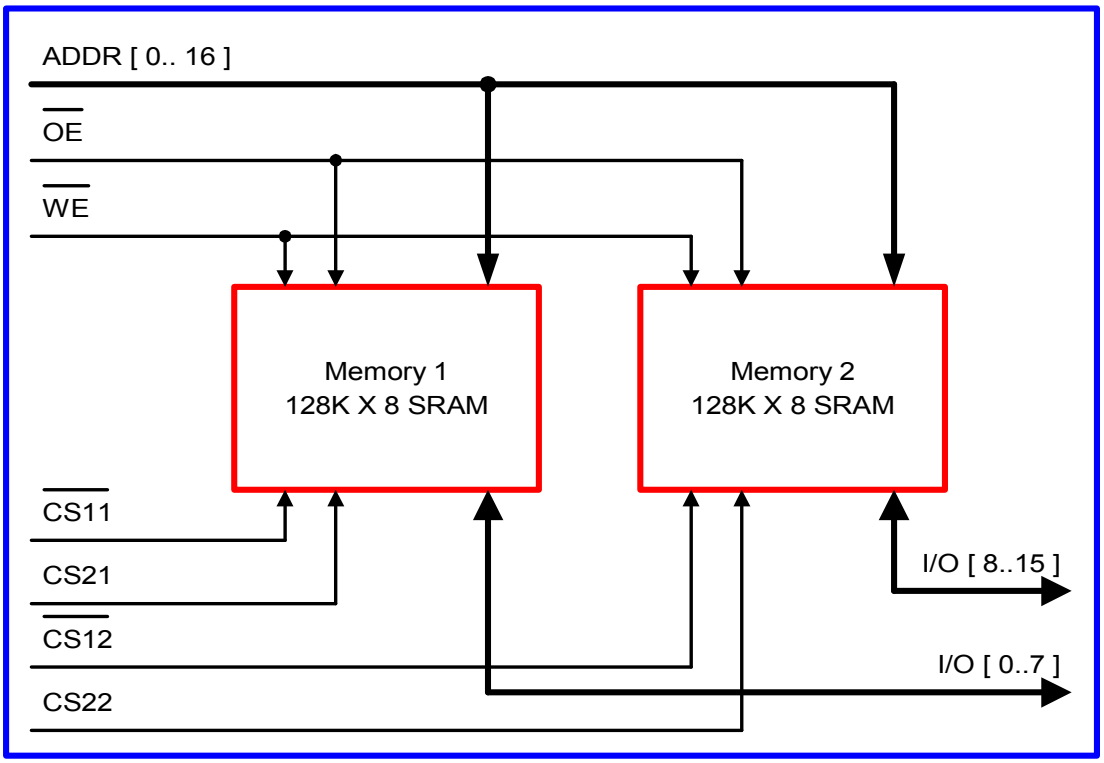
- High Temperature Digital Systems
- Petroleum LWD and MWD tools
- Petroleum reservoir monitoring

DESCRIPTION

The TX5304 is a CMOS static RAM organized as 131,072 x 16-bit words. The device is packaged in a proprietary 50-pin ceramic PGA package employing the 5 x 10 pin footprint with a pitch of 0.1 inch. Powered by a single +5 V supply, the unit offers low standby power dissipation and is suitable for battery backup systems. Three optional access times are available; output lines are tri-state; power consumption can be minimized through use of the data retention mode.

The TX5304 is composed of two individual SRAM modules, each with 128K x 8-bit memory. Each module has private enable/select lines permitting store/ access of either 8-bit or 16-bit data.

FUNCTIONAL BLOCK DIAGRAM



TX5304 -- Specifications

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage relative to V_{ss}	V_{cc}	-0.5 to + 5.5	V
Voltage on any pin relative to V_{ss}	V_T	-0.5 to Vcc + 0.5	V
Operating Temperature Range	T_{opr}	0 to + 200	ºC
Storage Temperature Range	T_{stg}	-55 to + 200	ºC

RECOMMENDED DC OPERATING CONDITIONS (Topr = 0 to +125ºC)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	4.5	5.5	V
	V_{ss}	0	0	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.2	V
Input Low Voltage	V_{IL}	-0.5	0.8	V

DC OPERATING CHARACTERISTICS (T_{opr} = 0 to +70ºC)

Parameter	Symbol	Typ	Unit
Input Leakage Current	I_{IN}	2.0	µA
Output Leakage Current	I_{OUT}	2.0	µA
Operating Supply Current	I_{CC}	70	mA
Standby Supply Current	I_{SB1}	4.0	mA
Data Retention Supply Current			
V_{cc} = 3.0	I_{DR}	0.2	uA
V_{cc} = 2.0	I_{DR}	0.2	uA
Output Voltage Low	V_{OL}	0.4	V
Output Voltage High	V_{OH}	2.4	V

TRUTH TABLE — For 128K x 16 bit operation

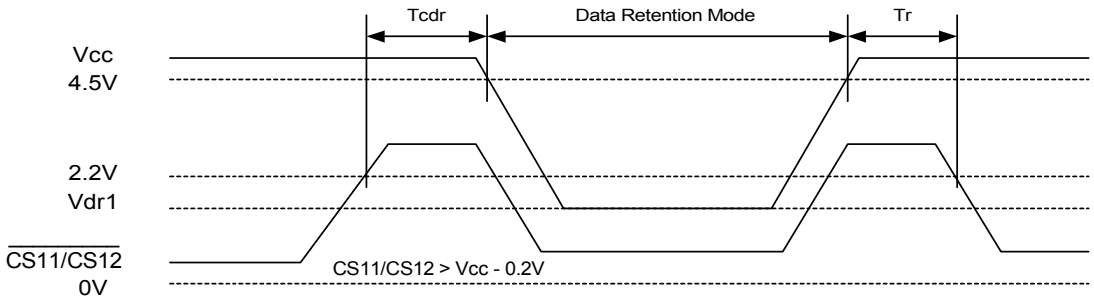
Mode	CS21/CS22	CS11/CS12	*WE	*OE	I/O Pin	Supply Current
Not Selected	L	X	X	X	High-Z	Standby
Not Selected	X	H	X	X	High-Z	Standby
Output Disable	H	L	H	H	High-Z	Active
Read	H	L	H	L	Data Output	Active
Write	H	L	L	X	Data Input	Active

H = High Voltage, L = Low Voltage, X = Don't Care

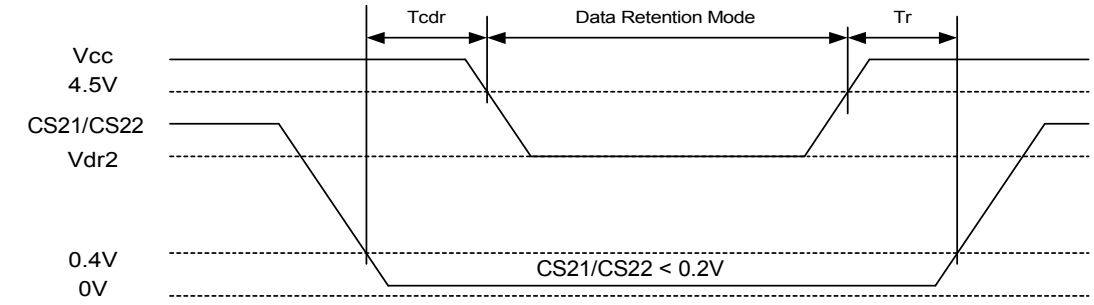
Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Typ	Unit
V_{CC} for data retention	V_{DR}	1.5	V
Chip deselect to data retention time	t_{CDR}	0	ns
Operation recovery time	t_{Rc}	100	ns

Low Vcc Data Retention Timing (CS11/CS21 Controlled)



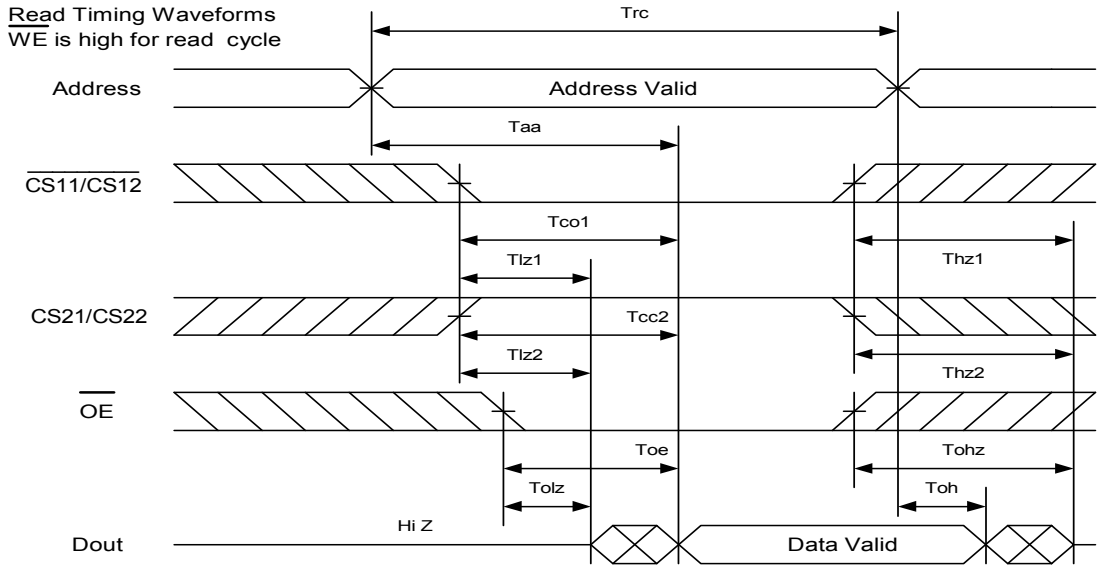
Low Vcc Data Retention Timing (CS21/CS22 Controlled)



TX5304 -- Specifications

AC OPERATING CHARACTERISTICS – *READ* CYCLE

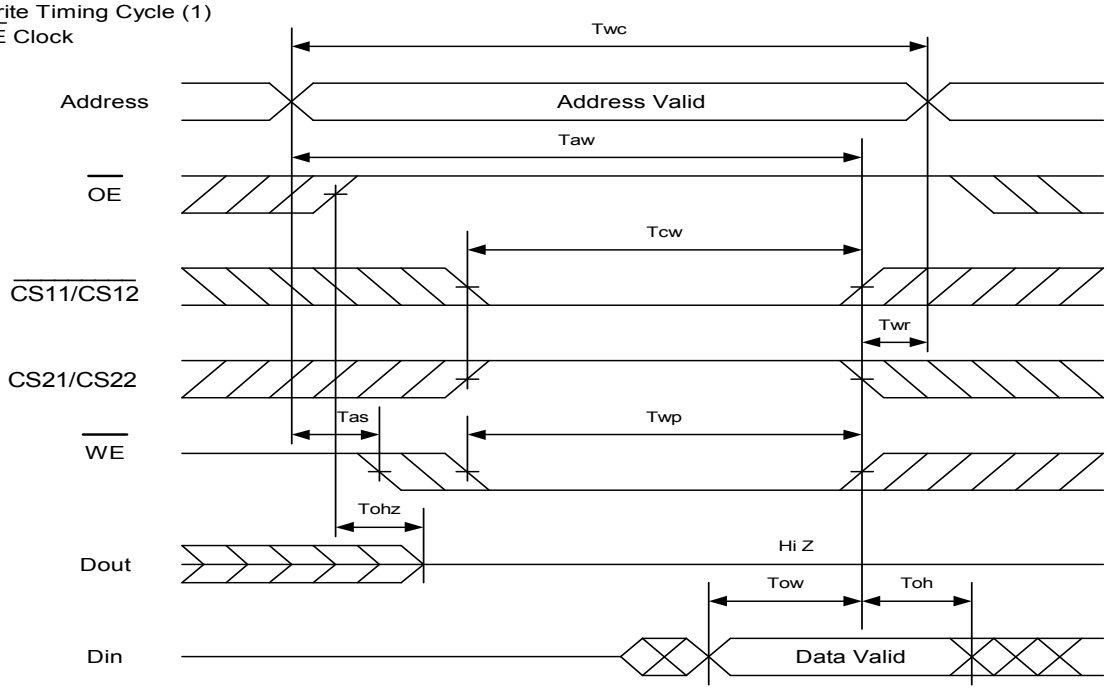
Parameter	Symbol	Min	Max	Unit	Notes
Read Cycle time	t_{RC}	100			ns
Address access time	t_{AA}		100		ns
Chip selecton to output valid	t_{CO}		100		ns
Output enable to output valid	t_{OE}		50		ns
Chip selection to output in low-Z	t_{LZ}	10			ns
Output enable to output in low-Z	t_{OZ}	10			ns
Output enable to output in high-Z	t_{HZ}		40		ns
Output disable to output in high-Z	t_{OHZ}		35		ns
Output hold from address change	t_{OH}	10			ns



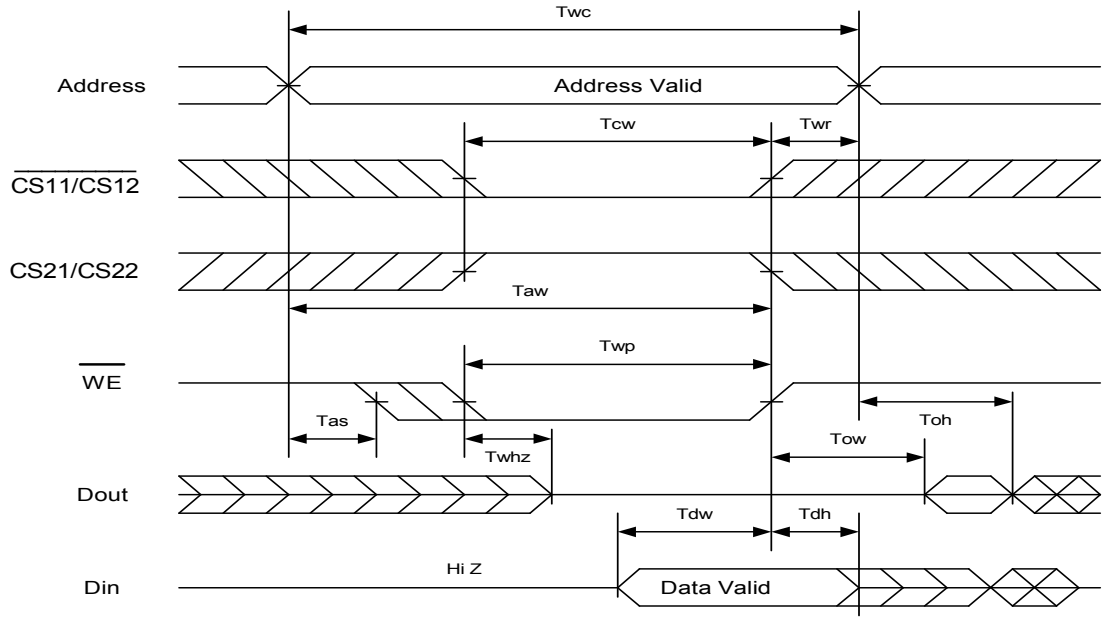
AC OPERATING CHARACTERISTICS – *WRITE* CYCLE

Parameter	Symbol	Typ	Max	Unit	Notes
Write Cycle time	t_{WC}	100		ns	
Chip selection time	t_{CW}	100		ns	
Address setup time	t_{AS}	0		ns	
Address valid to end of write	t_{AW}	100		ns	
Write pulse width	t_{WP}	50		ns	
Write recovery time	t_{WR}	0		ns	
Write to output in High-Z	t_{WHZ}	25	30	ns	
Data to write time overlap	t_{DW}	40		ns	
Data hold from write time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	5	30	ns	
Output disable to output in High-Z	t_{OHZ}	5		ns	

Write Timing Cycle (1)
OE Clock



Write Timing Cycle (2)
OE low fixed



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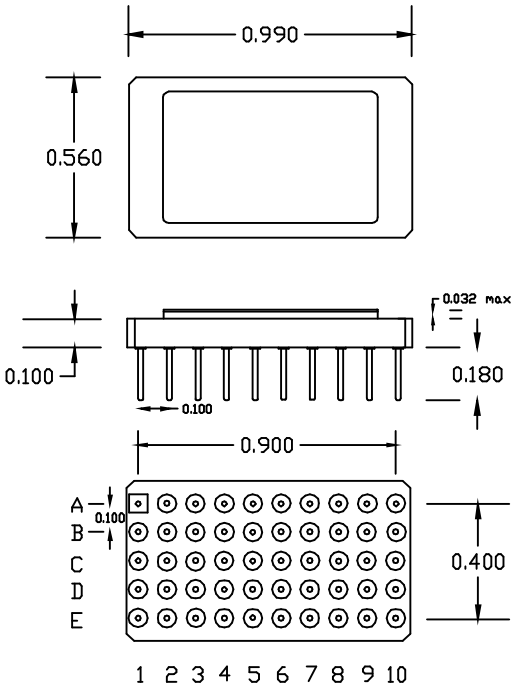
PACKAGE INFORMATION:



	A	B	C	D	E
1	N.C.	N.C.	N.C.	N.C.	$\overline{CS12}$
2	Vss	N.C.	N.C.	CS22	Vcc
3	N.C.	A16	$\overline{WE}$	CS21	A15
4	A14	A12	A7	A8	A13
5	A6	A5	$\overline{OE}$	A11	A9
6	A4	A3	A2	$\overline{CS11}$	A10
7	A1	A0	I/O13	I/O12	I/O11
8	I/O10	I/O9	I/O8	I/O15	I/O14
9	Vss	I/O1	I/O3	I/O5	Vcc
10	I/O0	I/O2	I/O4	I/O6	I/O7

WARNING! Static Sensitive Device.

The TX5304 is a hybrid network that includes several sensitive components. These components can be damaged or destroyed by discharge of static electricity. The discharge of static electricity is commonly referred to as Electrostatic Discharge (ESD).

The TX5304 can be protected from ESD by the following common procedures used with discrete semiconductors, namely:

1. Always store units in closed conductive containers
2. All personnel that handle units must wear static dissipative outer garments and must be electrically grounded
3. Always use a grounded soldering iron when making electrical connections
4. Worktables must have grounded dissipative covering.

ESD can cause subtle problems that have longer term, damaging affect.